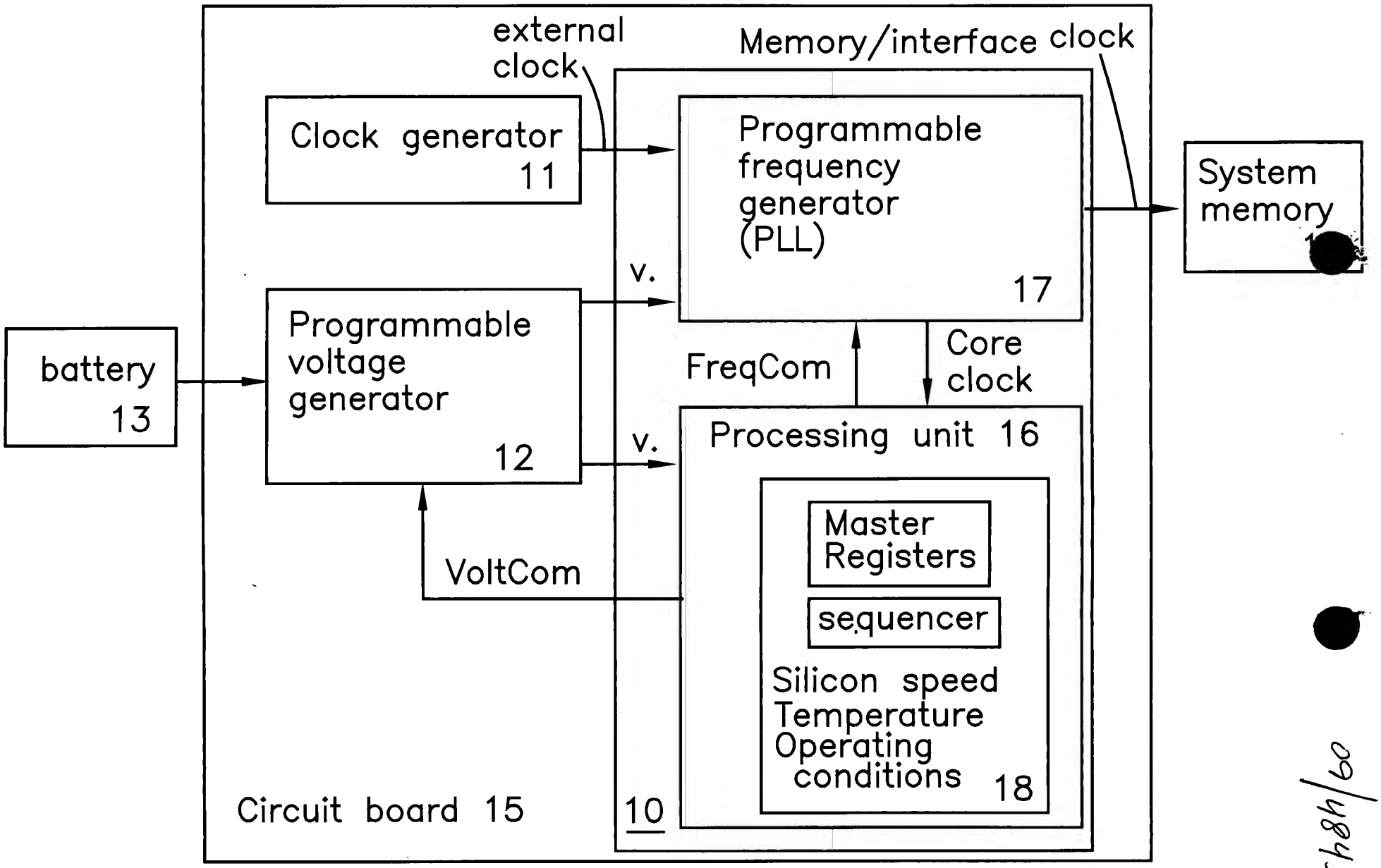


Figure 1

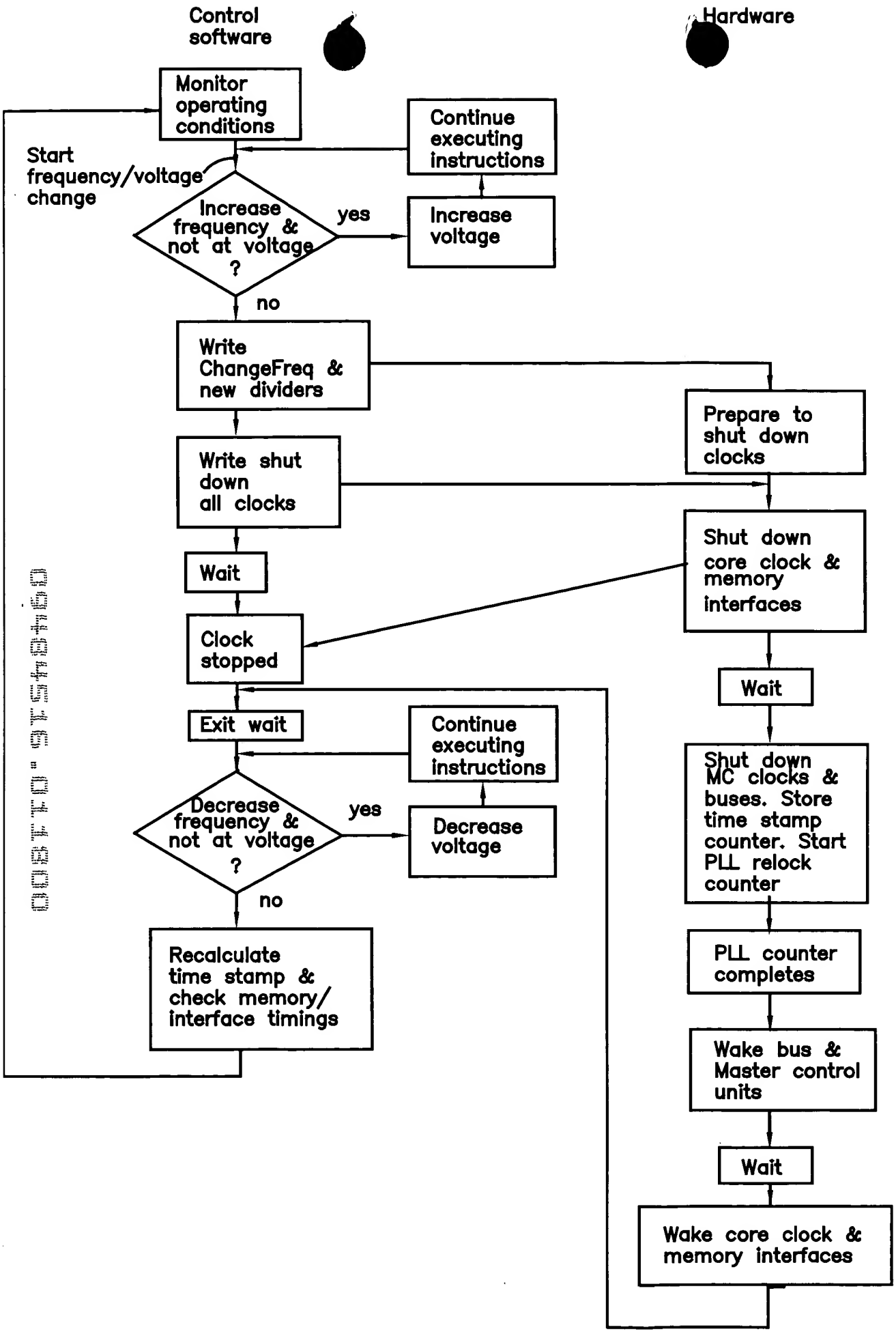
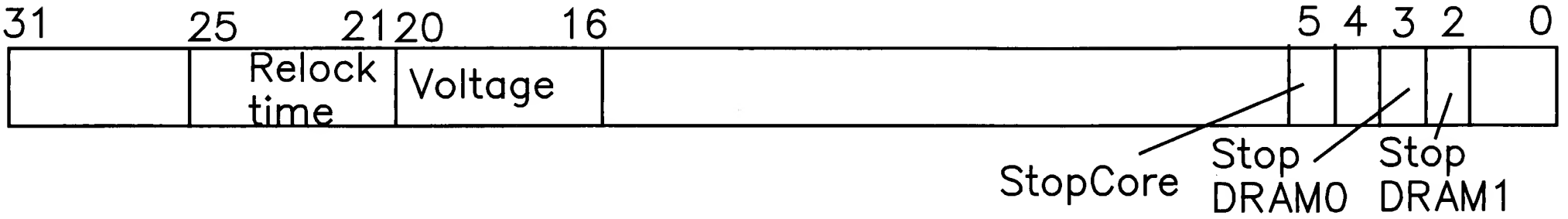
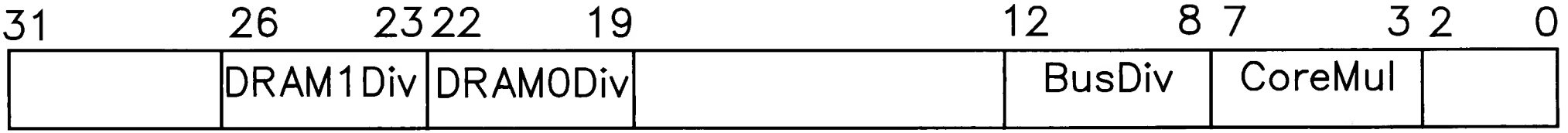

Control software
Hardware
Monitor operating conditions
Continue executing instructions
Start frequency/voltage change
Increase frequency & not at voltage ?
yes
Increase voltage
no
Write ChangeFreq & new dividers
Prepare to shut down clocks
Write shut down all clocks
Shut down core clock & memory interfaces
Wait
Clock stopped
Wait
Exit wait
Continue executing instructions
Shut down MC clocks & buses. Store time stamp counter. Start PLL relock counter
Decrease frequency & not at voltage ?
yes
Decrease voltage
no
Recalculate time stamp & check memory/ interface timings
PLL counter completes
Wake bus & Master control units
Wait
Wake core clock & memory interfaces

Figure 2

Master Control Register



Master Status Register



Clock Divider Register

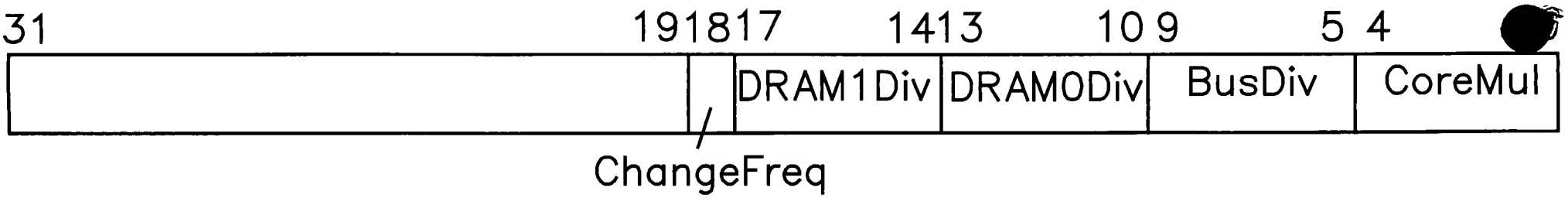


Figure 3

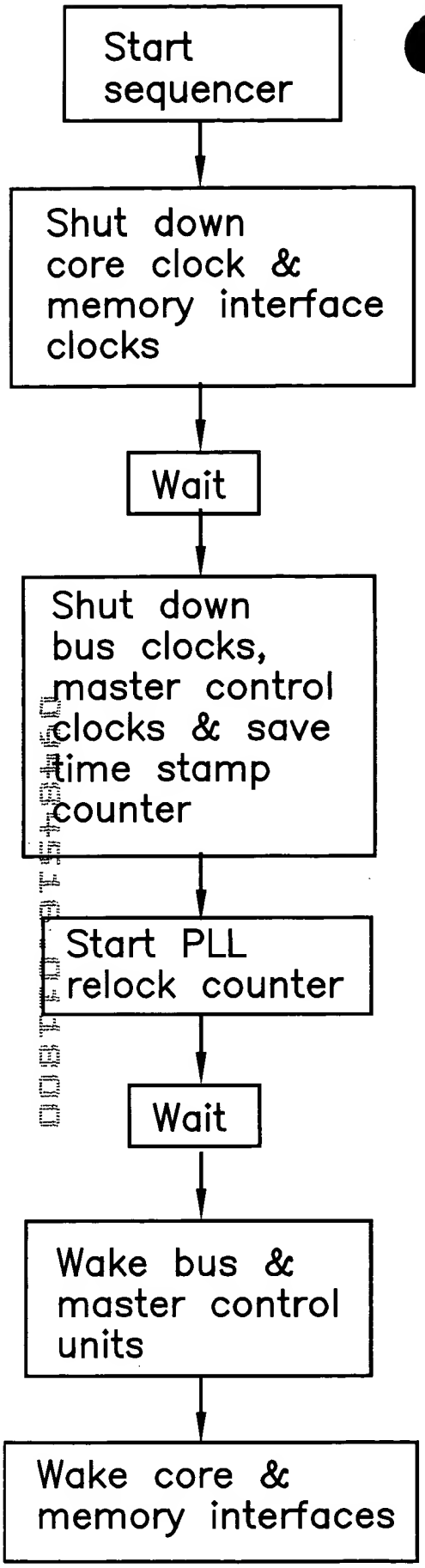

Start sequencer
Shut down core clock & memory interface clocks
Wait
Shut down bus clocks, master control clocks & save time stamp counter
Start PLL relock counter
Wait
Wake bus & master control units
Wake core & memory interfaces

Figure 4